ABSTRACT

A compiler which improves the processing speed of a program execution without needlessly issuing an instruction that has a possibility of causing an interlock is targeted at a processor having an instruction that has a possibility of causing an interlock when the instruction is executed, the compiler causing a computer to function as: a loop structure transforming unit (186) which performs double looping transformation on an input program so that a loop whose iteration count is y is split off from a loop whose loop count is x and the loop whose iteration count is y is an inner loop whereas a loop whose iteration count is x/y is an outer loop; and an instruction optimum placing unit (187) which places an instruction that has a possibility of causing an interlock in the program on which the double looping transformation has been performed.